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EXAMINER	
GREY, CHRISTOPHER P	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/649,315	SINGH ET AL.	
	Examiner	Art Unit	
	CHRISTOPHER P. GREY	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-17,19-22 and 24-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,10-17,19-22 and 24-33* is/are rejected.

7)☒ Claim(s) *7-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the appeal brief filed on 12/12/08, PROSECUTION IS HEREBY REOPENED. A new grounds of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Response to Amendment

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

In view of applicant's amendment filed on 12/12/08, the status of the application is still pending with respect to claims 1, 3-17, 19-22 and 24-33.

Response to Arguments

3. Applicant's arguments, see appeal brief, filed on 12/12/08, with respect to all the claims have been fully considered and are persuasive. The finality (rejection) of these claims has been withdrawn.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 12, 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (US 2004/0059766) in view of the applicants admitted prior art.

Regarding Claim 1, Yeh discloses an inverse fast Fourier transform circuit **(see fig 10 which shows and IFFT circuit, notice IFFT control circuit 606)** having a length of N samples **(fig 13 and Para 0076 shows that the IFFT circuit is a 128 point circuit where 128= 2^7, where N is equivalent to 7 and can also be equivalent to any number of samples depending on a designers preference)**, the inverse fast Fourier transform circuit **(see fig 10 which shows and IFFT circuit, notice IFFT control circuit 606)** adapted to receive input data of length N samples **(fig 10 shows input X (k), where N can be any number of samples including the number of samples within the input X (k))**, to circularly shift **(fig 8 shows a complex rotator which is a part of the IFFT circuit shown in fig 10, where the complex rotator of fig 8 shows a pie/2 rotator, where pie/2 is equivalent to a portion of a circle, thus**

circular rotation occurs in 503 and is followed by right shifting in 505, thus the combination making up a circular shift) the input data **(fig 10 and 8 see input X (k))** by m samples **(fig 8, where there exists 5 right shifters, where 5 or any number associated with the circular shifting is equivalent to m)**; and generate output data of length N samples **(see input and output of complex rotator of fig 8, where if k is the length, k is present in the input and output, and is equivalent to N)** that are circularly shifted by m samples **(fig 8, where there exists 5 right shifters, where 5 or any number associated with the circular shifting is equivalent to m)**.

Yeh does not specifically disclose a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m, the cyclical prefix insertion circuit having;

1. a first switch connected to the inverse fast Fourier transform circuit.

2. a buffer having an input connected to the first switch and an output, the buffer having a length m.

3. a second coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch.

The applicants admitted prior art discloses a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m **(page 7, Para 0037 and see fig 3, GI represents guard interval and Para 0036 discloses a length of 16)**, the cyclical prefix insertion circuit having;

1. a first switch (fig 3, 126), connected to the inverse fast Fourier transform circuit **(fig 3, IFFT output).**

2. a buffer (fig 3, 128), having an input connected to the first switch **(fig 3, 126)** and an output, the buffer having a length m **(Para 0036 discloses length of 16).**

3. a second switch **(fig 3, 130)**, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch **(see fig 3 for details).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention modify the IFFT circuit of Yeh, as taught by the AAPA, since stated in Para 0037 that such a modification will improve selectively routing of the output of the IFFT.

Regarding claim 12, Yeh discloses an OFDM system (Para 0004 OFDM).

Regarding Claim 17, Yeh discloses a means **(fig 3, 37 and 36 make up the means)** for performing a circularly shifted **(Para 0058, where the complex rotator indicates circular shifting present)** IFFT on frequency domain information **(fig 3, X(k), where IFFT circuit indicates transform of frequency domain to time domain)** to generate time domain information , wherein the circular shift is approximately the same as a desired cyclical prefix and input samples for the IFFT are not multiplied by rotator coefficients **(see fig 3, where Butterfly circuits and Radix algorithm alleviate the need for multiplying input X(k). Furthermore, the Radix format does not require elements 202 and 206 of fig 12 as argued by the applicant)** and the N samples are not multiplied by rotator coefficients **(fig 8, where circular shifting occurs within fig 8 which shows a complex rotator which is a part of the IFFT circuit shown in fig 10, where the complex rotator of fig 8 shows a pie/2 rotator, where pie/2 is equivalent**

to a portion of a circle, thus circular rotation occurs in 503 and is followed by right shifting in 505, thus the combination making up a circular shift, and there exists no multipliers) .

Yeh does not specifically a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m, the cyclical prefix insertion circuit having;

1. a first switch connected to the inverse fast Fourier transform circuit.

2. a buffer having an input connected to the first switch and an output, the buffer having a length m.

3. a second coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch.

The applicants admitted prior art discloses a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m **(page 7, Para 0037 and see fig 3, GI represents guard interval and Para 0036 discloses a length of 16)**, the cyclical prefix insertion circuit having;

1. a first switch (fig 3, 126), connected to the inverse fast Fourier transform circuit **(fig 3, IFFT output).**

2. a buffer (fig 3, 128), having an input connected to the first switch **(fig 3, 126)** and an output, the buffer having a length m **(Para 0036 discloses length of 16).**

3. a second switch **(fig 3, 130)**, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the

inverse fast Fourier transform circuit to an output of the second switch **(see fig 3 for details).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention modify the IFFT circuit of Yeh, as taught by the AAPA, since stated in Para 0037 that such a modification will improve selectively routing of the output of the IFFT.

Regarding claim 19, Yeh disclose wherein the IFFT circuit (see fig 10) further comprises a plurality of butterfly circuits (fig 10 and 13 show BF's), multiplier circuits (fig 10 and 13 shows multipliers) with memory (fig 10 and 13 shows incoming signal connected to multiplier, where some form of memory must exist) and rotator circuits (fig 8 shows rotator circuits), all coupled to a control circuit (figs 10 and 13 show control circuit) and wherein the IFFT is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits (fig 10 and 13, notice that the control unit sends a signal to the memory for making a modification to the multiplier) with memory (fig 10 and 13 where the control unit and memory are coupled together and must contain some form of memory for performing logical operations) and modifying the control for the rotator circuits (fig 8, where the rotator is modified by the insertion of data X(k). the claim does not define what form of modification is made).

Regarding claim 20, Yeh disclose wherein the IFFT circuit (see fig 10) further comprises a plurality of butterfly circuits (fig 10 and 13 show BF's), multiplier circuits (fig 10 and 13 shows multipliers) with memory (fig 10 and 13 shows incoming signal connected to multiplier, where some form of memory must exist) and rotator circuits (fig 8 shows rotator circuits), all coupled to a control circuit (figs 10 and 13 show control

circuit) and wherein the IFFT is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits (fig 10 and 13, notice that the control unit sends a signal to the memory for making a modification to the multiplier) with memory (fig 10 and 13 where the control unit and memory are coupled together and must contain some form of memory for performing logical operations) and modifying the control for the rotator circuits (fig 8, where the rotator is modified by the insertion of data X(k). the claim does not define what form of modification is made).

Regarding claim 21, Yeh discloses an OFDM system (Para 0004 OFDM).

6. Claims 3-6, 10, 11, 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (US 2004/0059766) in view of the applicants admitted prior art, in further view of Walton et al. (US 20040081131), hereinafter referred to as Walton

Regarding claim 3, Yeh discloses wherein the length of N samples is a power of 2 **(see Para 0076 for 128=2^7)** and wherein the IFFT circuit **(see fig 10 which shows and IFFT circuit, notice IFFT control circuit 606)** implements an algorithm **(Para 0076 shows a radix algorithm)**

The combined teaching of Yeh and AAPA do not specifically disclose selected from the group consisting of Radix-2 and Radix 2^2 algorithms.

Walton discloses selected from the group consisting of Radix-2 and Radix 2^2 algorithms **(Para 0044 and Para 0042 where Nmax= 2^S)**.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the IFFT unit as disclosed by the combined teachings of Yeh and

the applicants admitted prior art to employ a decimation in time or decimation in frequency IFFT algorithm (Para 0044). The motivation for this modification is to allow IFFT of different sizes to be performed using a single IFFT unit.

Regarding claim 4, Yeh disclose wherein the IFFT circuit (see fig 10) further comprises a plurality of butterfly circuits (fig 10 and 13 show BF's), multiplier circuits (fig 10 and 13 shows multipliers) with memory (fig 10 and 13 shows incoming signal connected to multiplier, where some form of memory must exist) and rotator circuits (fig 8 shows rotator circuits), all coupled to a control circuit (figs 10 and 13 show control circuit) and wherein the IFFT is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits (fig 10 and 13, notice that the control unit sends a signal to the memory for making a modification to the multiplier) with memory (fig 10 and 13 where the control unit and memory are coupled together and must contain some form of memory for performing logical operations) and modifying the control for the rotator circuits (fig 8, where the rotator is modified by the insertion of data X(k). the claim does not define what form of modification is made).

Regarding claim 5, Yeh disclose wherein the IFFT circuit (see fig 10) further comprises a plurality of butterfly circuits (fig 10 and 13 show BF's), multiplier circuits (fig 10 and 13 shows multipliers) with memory (fig 10 and 13 shows incoming signal connected to multiplier, where some form of memory must exist) and rotator circuits (fig 8 shows rotator circuits), all coupled to a control circuit (figs 10 and 13 show control circuit) and wherein the IFFT is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits (fig 10 and 13, notice that the

control unit sends a signal to the memory for making a modification to the multiplier) with memory (fig 10 and 13 where the control unit and memory are coupled together and must contain some form of memory for performing logical operations) and modifying the control for the rotator circuits (fig 8, where the rotator is modified by the insertion of data X(k). the claim does not define what form of modification is made).

Regarding claim 6, Yeh discloses a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits and coupled to an input (see figs 10 and 13 for circuits), wherein each butterfly circuit is configured to perform and addition operation and a subtraction operation (see fig 4 for BF with adder and subtractor);

A control circuit (fig 3 36) configured to modify the control to the rotator circuit (fig 3, notice control circuit sends control signals to BFs) and to selectively control the plurality of butterfly circuits (fig 3, notice control circuit sends control signals to BFs) whether the addition operation or the subtraction operation is output first in time (fig 4, notice 106 is control signal to control output of MUX's) to effect a circular shift of the output of the IFFT circuit by m samples (circular shifting is discussed within the rejection of claim 1)

The contents of the memory of the multiplier circuit with memory are arranged in a suitably modified manner (fig 3, see multiplier and control unit acts as memory and controls/modifies the input thereof).

Regarding claim 10, Yeh discloses wherein the length of N samples ~~coefficients~~ of the Inverse Fast Fourier Transform and the cyclical prefix has a length m equal to N/4, and a control for a first rotator circuit is modified to effect the shift of the samples at

the output of the Inverse Fast Fourier Transform by m samples (see fig 3, where BF's are controlled by control circuit)

Regarding claim 11, The combined teachings of Yeh does not specifically disclose wherein the length of N coefficients of the IFFT is equal to 64 and the cyclical prefix has a length m equal to 16, and the modification is applied to control for the first rotator circuit of the IFFT circuit to circularly shift the output data by 16 coefficients.

AAPA discloses wherein the length of N coefficients of the IFFT is equal to 64 and the cyclical prefix has a length m equal to 16, and the modification is applied to control for the first rotator circuit of the IFFT circuit to circularly shift the output data by 16 coefficients.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the switches as disclosed by fig 3 of the admitted prior art within the circuit provided in fig 4, 20 of Mazzino. The motivation for this combination is to selectively route the output of the IFFT.

Regarding Claim 13, Yeh discloses a transform circuit wherein the length of N samples is a power of 2 **(Para 0052, N=2^n)** and the N samples are not multiplied by rotator coefficients **(fig 8, where circular shifting occurs within fig 8 which shows a complex rotator which is a part of the IFFT circuit shown in fig 10, where the complex rotator of fig 8 shows a pie/2 rotator, where pie/2 is equivalent to a portion of a circle, thus circular rotation occurs in 503 and is followed by right shifting in 505, thus the combination making up a circular shift, and there exists no multipliers)**

circularly shifting by m samples **(fig 8, where there exists 5 right shifters, where 5 or any number associated with the circular shifting is equivalent to m)**

Yeh discloses the transform circuit further having a plurality of butterfly circuits **(fig 3, 31-33)**, multiplier circuits **(fig 3, 38)** with memory and rotator circuits **(Para 0058)**, all coupled to a control circuit **(fig 3, 36),** wherein an output of the transform circuit is modifying the control to a first stage rotator circuit and modifying the memory contents of the multiplier circuit, where m is less than N **(Para 0071).**

Yeh does not specifically disclose a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m, the cyclical prefix insertion circuit having;

1. a first switch connected to the inverse fast Fourier transform circuit.

2. a buffer having an input connected to the first switch and an output, the buffer having a length m.

3. a second coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch.

The applicants admitted prior art discloses a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m **(page 7, Para 0037 and see fig 3, GI represents guard interval and Para 0036 discloses a length of 16)**, the cyclical prefix insertion circuit having;

1. a first switch (fig 3, 126), connected to the inverse fast Fourier transform circuit **(fig 3, IFFT output).**

2. a buffer (fig 3, 128), having an input connected to the first switch **(fig 3, 126)** and an output, the buffer having a length m **(Para 0036 discloses length of 16).**

3. a second switch **(fig 3, 130)**, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch **(see fig 3 for details).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention modify the IFFT circuit of Yeh, as taught by the AAPA, since stated in Para 0037 that such a modification will improve selectively routing of the output of the IFFT.

The combined teaching of Yeh and AAPA do not specifically disclose selected from the group consisting of Radix-2 and Radix 2^2 algorithms.

Walton discloses selected from the group consisting of Radix-2 and Radix 2^2 algorithms **(Para 0044 and Para 0042 where Nmax= 2^S)**.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the IFFT unit as disclosed by the combined teachings of Yeh and the applicants admitted prior art to employ a decimation in time or decimation in frequency IFFT algorithm (Para 0044). The motivation for this modification is to allow IFFT of different sizes to be performed using a single IFFT unit.

Regarding claim 14, Yeh disclose wherein the IFFT is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits (fig 10 and 13, notice that the control unit sends a signal to the memory for making a modification to the multiplier) with memory (fig 10 and 13 where the control unit and

memory are coupled together and must contain some form of memory for performing logical operations) and modifying the control for the rotator circuits (fig 8, where the rotator is modified by the insertion of data X(k). the claim does not define what form of modification is made).

Regarding claim 15, Yeh disclose wherein the IFFT is adapted to circularly shift the input data by m samples by modifying the order of the memory contents for multiplier circuits (fig 10 and 13, notice that the control unit sends a signal to the memory for making a modification to the multiplier) with memory (fig 10 and 13 where the control unit and memory are coupled together and must contain some form of memory for performing logical operations) and modifying the control for the rotator circuits (fig 8, where the rotator is modified by the insertion of data X(k). the claim does not define what form of modification is made) and butterfly circuits, (notice control unit sends control to BF's in fig 3).

Regarding claim 16, Yeh discloses the modification is applied to control for the first rotator circuit of the IFFT circuit to circularly shift the output data by 16 samples (fig 8, where shifting of 16 bits using 505 a-c and e circularly shifts 16 bits, where each bit is made equivalent to a sample)

The combined teachings of Yeh does not specifically disclose wherein the length of N coefficients of the IFFT is equal to 64 and the cyclical prefix has a length m equal to 16, and the modification is applied to control for the first rotator circuit of the IFFT circuit to circularly shift the output data by 16 coefficients.

AAPA discloses wherein the length of N coefficients of the IFFT is equal to 64 and the cyclical prefix has a length m equal to 16, and the modification is applied to control for the first rotator circuit of the IFFT circuit to circularly shift the output data by 16 coefficients.

It would have been obvious to one of the ordinary skill in the art at the time of the invention modify the IFFT circuit of Yeh, as taught by the AAPA, since stated in Para 0037 that such a modification will improve selectively routing of the output of the IFFT.

7. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (US 2004/0059766) in view of Mazzino (US 20040151110) in view of the applicants admitted prior art.

Regarding claim 22, Yeh discloses a. performing a circularly rotated **(Para 0058, where the complex rotator indicates circular shifting present)** Inverse Fast Fourier Transform **(see fig 10 which shows and IFFT circuit, notice IFFT control circuit 606)** on frequency domain information (fig 3 x k) to generate time domain information (x n) without multiplying input samples by rotator coefficients **(fig 8, where circular shifting occurs within fig 8 which shows a complex rotator which is a part of the IFFT circuit shown in fig 10, where the complex rotator of fig 8 shows a pie/2 rotator, where pie/2 is equivalent to a portion of a circle, thus circular rotation occurs in 503 and is followed by right shifting in 505, thus the combination making up a circular shift, and there exists no multipliers)**,

Yeh does not specifically disclose wherein the amount of the circular shift is the same as the length of the cyclical prefix; b. storing the time domain information for a number of clock cycles equal to the cyclical prefix in a buffer while simultaneously outputting the time domain information; c. outputting the time domain information for a number of clock cycles equal to a length of the Inverse Fast Fourier Transform minus the length of the cyclical prefix; and d. outputting the time domain information stored in the buffer for a number of clock cycles equal to the length of the cyclical prefix.

Mazzino wherein the amount of the circular shift is the same as the length of the cyclical prefix **(Para 0031, circular shifting samples of a symbol so that the last samples forming the symbol before shifting form the prefix).**

(b) storing the time domain for a number of clock cycles equal to the cyclical prefix in a buffer (Para 0037, samples stored in memory in fig 3, 24) while simultaneously outputting the time domain information **(Para 0038, provides first sample; store the samples generated by IFFT).**

(d) outputting the time domain information stored in the buffer for a number of clock cycles equal to the length of the cyclical prefix **(Para 0040, where memory is controlled in the read mode at a time).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention was disclosed to modify the IFFT circuit of Yeh, as taught by Mazzino, since stated in Para 0017 that such a modification reduces delay.

The combined teachings of Yeh and Mazzino do not specifically disclose (c) outputting the time domain information for a number of clock cycles equal to a length of the IFFT minus the length of the cyclical prefix.

The applicants admitted prior art discloses (c) outputting the time domain information for a number of clock cycles equal to a length of the IFFT minus the length of the cyclical prefix **(Para 0037, the samples 0 to 63 will then be read out of the buffer).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention modify the IFFT circuit of the combined teachings of Yeh and Mazzino, as taught by the AAPA, since stated in Para 0037 that such a modification will improve selectively routing of the output of the IFFT.

Regarding claim 24, Yeh disclose wherein the IFFT circuit (see fig 10) further comprises a plurality of butterfly circuits (fig 10 and 13 show BF's), multiplier circuits (fig 10 and 13 shows multipliers) with memory (fig 10 and 13 shows incoming signal connected to multiplier, where some form of memory must exist) and rotator circuits (fig 8 shows rotator circuits), all coupled to a control circuit (figs 10 and 13 show control circuit) and wherein the IFFT is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits (fig 10 and 13, notice that the control unit sends a signal to the memory for making a modification to the multiplier) with memory (fig 10 and 13 where the control unit and memory are coupled together and must contain some form of memory for performing logical operations) and

modifying the control for the rotator circuits (fig 8, where the rotator is modified by the insertion of data X(k). the claim does not define what form of modification is made).

Regarding claim 25, Yeh disclose wherein the IFFT circuit (see fig 10) further comprises a plurality of butterfly circuits (fig 10 and 13 show BF's), multiplier circuits (fig 10 and 13 shows multipliers) with memory (fig 10 and 13 shows incoming signal connected to multiplier, where some form of memory must exist) and rotator circuits (fig 8 shows rotator circuits), all coupled to a control circuit (figs 10 and 13 show control circuit) and wherein the IFFT is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits (fig 10 and 13, notice that the control unit sends a signal to the memory for making a modification to the multiplier) with memory (fig 10 and 13 where the control unit and memory are coupled together and must contain some form of memory for performing logical operations) and modifying the control for the rotator circuits (fig 8, where the rotator is modified by the insertion of data X(k). the claim does not define what form of modification is made).

8. Claims 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (US 2004/0059766) in view of Walton et al. (US 20040081131), hereinafter referred to as Walton.

Regarding claim 26, Yeh discloses a transform circuit having a length of N samples (fig 3, shows a transform circuit), where N is a power of 2 (N can be any number), the transform circuit further having a plurality of butterfly circuits (fig 13, see butterfly circuits), multiplier circuits (fig 13, see multipliers) with memory (fig 13, see

coefficients and step count which require memory for storing these values) and rotator circuits (fig 8, where the butterfly circuits consist of rotator circuits 503), all coupled to a control circuit (fig 3, 806), wherein an output of the transform circuit is circularly shifted by m samples (fig 5, shows circular shifting by m samples, m being an unspecified number as claimed) by modifying the control to a first stage rotator circuit (fig 5, modification are made to the control signals 206 to the rotator circuit of fig 5) and modifying the memory contents of the multiplier circuit (fig 13, shows modifications being made to the multiplier via a control signal from the control unit), where m is less than N (m is known to be less than N).

Yeh does not specifically disclose implementing an algorithm selected from the group consisting of Radix-2 and Radix-22 algorithms.

Walton discloses selected from the group consisting of Radix-2 and Radix 2^2 algorithms **(Para 0044 and Para 0042 where Nmax= 2^S)**.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the IFFT unit as disclosed by the teachings of Yeh to employ a decimation in time or decimation in frequency IFFT algorithm (Para 0044). The motivation for this modification is to allow IFFT of different sizes to be performed using a single IFFT unit.

Regarding claim 27, Yeh discloses wherein the transform circuit comprises a Fast Fourier Transform circuit (fig 16, shows FFT circuit).

Regarding claim 28, Yeh discloses wherein the transform circuit comprises an Inverse Fast Fourier Transform circuit (fig 16, IFFT circuit).

Regarding claim 29, Yeh discloses wherein the transform circuit is configurable as an Inverse Fast Fourier Transform circuit and as a Fast Fourier Transform circuit, wherein each configuration maintains the same circular shift of m samples (fig 3, shows both IFFT and FFT, and both used the same circuitry for circular shifting).

Regarding claim 30, Yeh discloses a transform circuit having a length of N samples (fig 3, shows a transform circuit), where N is a power of 2 (N can be any number), the transform circuit further having a plurality of butterfly circuits (fig 13, see butterfly circuits), multiplier circuits (fig 13, see multipliers) with memory (fig 13, see coefficients and step count which require memory for storing these values) and rotator circuits (fig 8, where the butterfly circuits consist of rotator circuits 503), all coupled to a control circuit (fig 3, 806), wherein an output of the transform circuit is circularly shifted by m samples (fig 5, shows circular shifting by m samples, m being an unspecified number as claimed) by modifying the control to the butterfly circuit (fig 13, shows control signals modifying the butterfly circuits), modifying the control to the rotator circuit (fig 5, modification are made to the control signals 206 to the rotator circuit of fig 5) and re-ordering the memory contents of the multiplier circuit (fig 13, shows modifications being made to the multiplier via a control signal from the control unit), where m is less than N (m is known to be less than N).

Yeh does not specifically disclose implementing an algorithm selected from the group consisting of Radix-2 and Radix-22 algorithms.

Walton discloses selected from the group consisting of Radix-2 and Radix 2^2 algorithms **(Para 0044 and Para 0042 where Nmax= 2^S)**.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the IFFT unit as disclosed by the teachings of Yeh to employ a decimation in time or decimation in frequency IFFT algorithm (Para 0044). The motivation for this modification is to allow IFFT of different sizes to be performed using a single IFFT unit.

Regarding claim 31, Yeh discloses wherein the transform circuit comprises a Fast Fourier Transform circuit (fig 16, shows FFT circuit).

Regarding claim 32, Yeh discloses wherein the transform circuit comprises an Inverse Fast Fourier Transform circuit (fig 16, IFFT circuit).

Regarding claim 33, Yeh discloses wherein the transform circuit is configurable as an Inverse Fast Fourier Transform circuit and as a Fast Fourier Transform circuit, wherein each configuration maintains the same circular shift of m samples (fig 3, shows both IFFT and FFT, and both used the same circuitry for circular shifting).

Allowable Subject Matter

7. Claims 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims, as the closest prior art of record does not specifically disclose the length of the samples being segmented into 4 segments, where the circular shift m is equal to N/4 and the N samples is multiplied by -1, -j, j and unity.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER P. GREY whose telephone number is (571)272-3160. The examiner can normally be reached on 10AM-7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Moe Aung can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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